Fig. 1

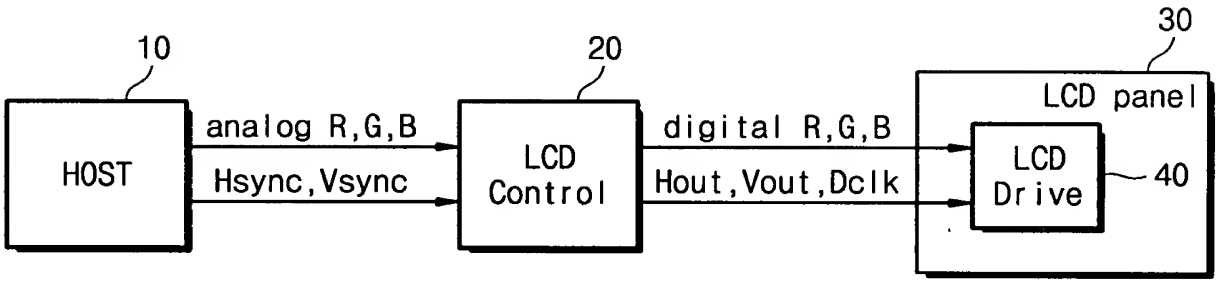

10
20
30
HOST
analog R,G,B
Hsync,Vsync
LCD Control
digital R,G,B
Hout,Vout,Dclk
LCD panel
LCD Drive
40

Fig. 2

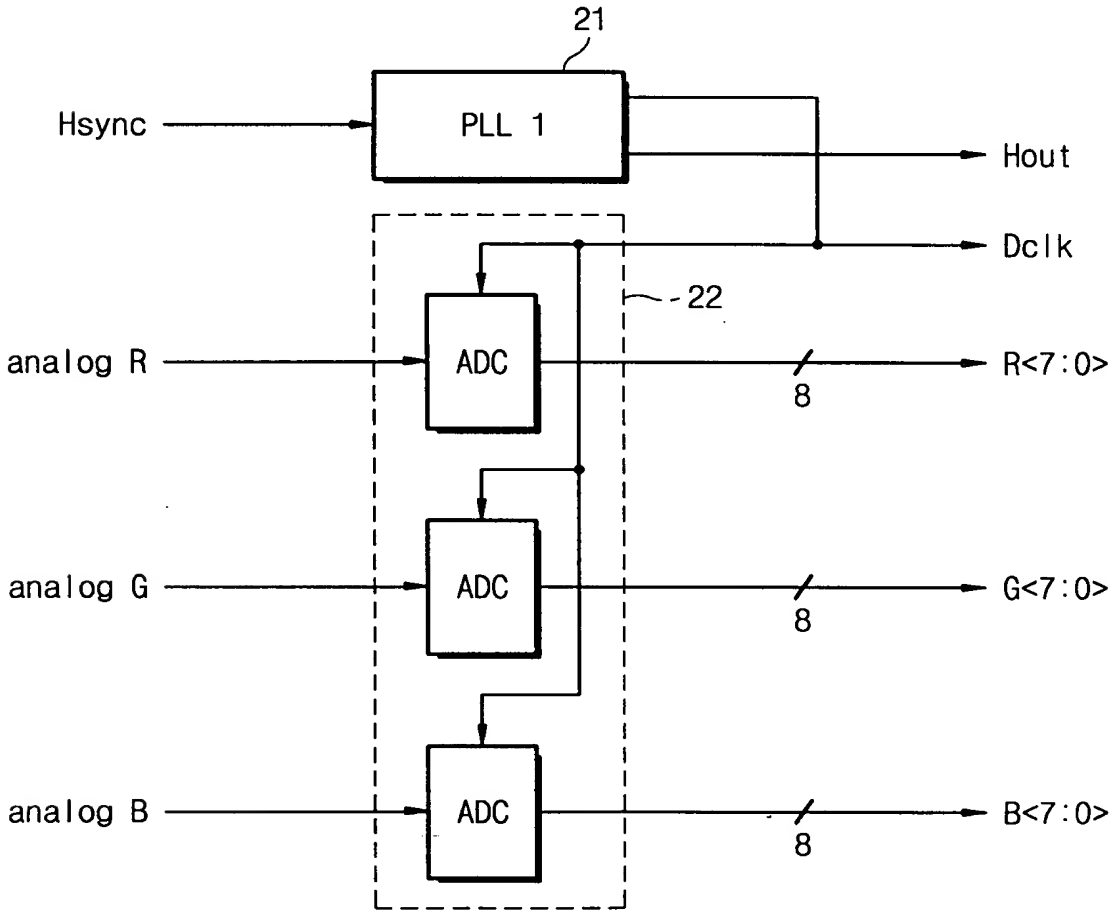

21
Hsync
PLL 1
Hout
Dclk
22
analog R
ADC
8
R<7:0>
analog G
ADC
8
G<7:0>
analog B
ADC
8
B<7:0>

Fig. 3

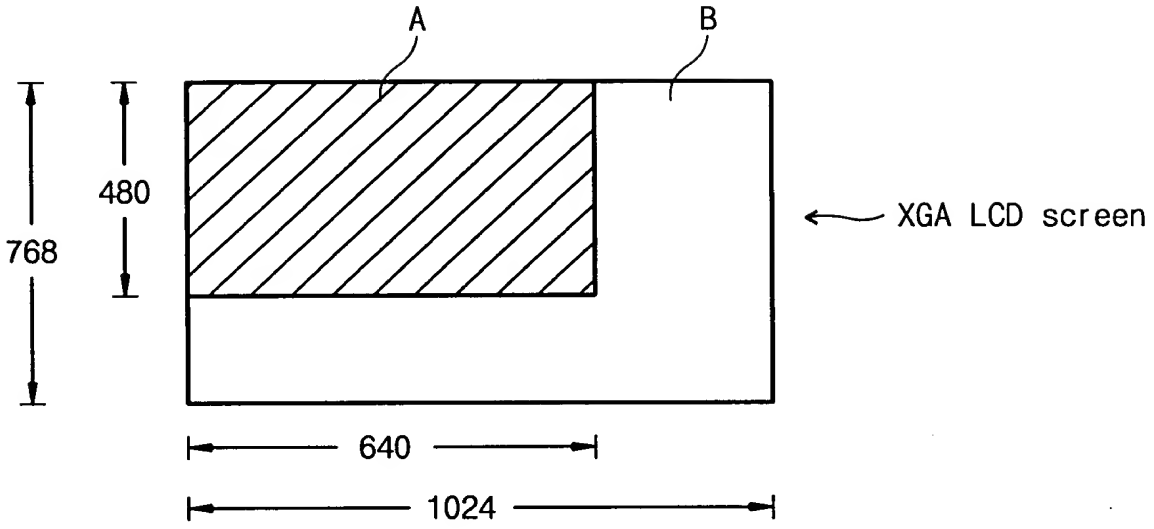

A
B
480
768
XGA LCD screen
640
1024

Fig. 4

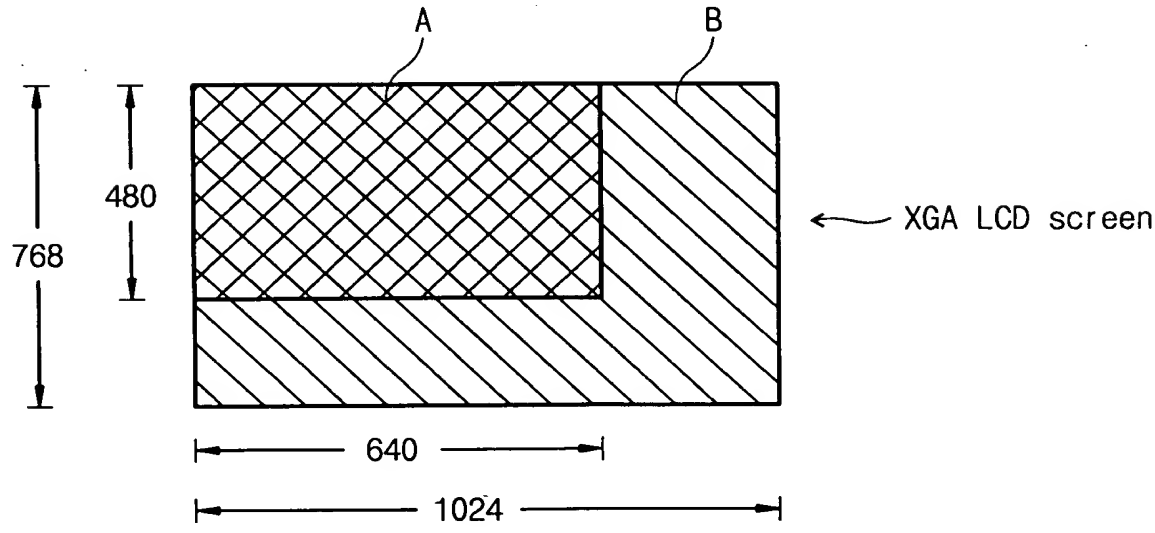

A
B
480
768
XGA LCD screen
640
1024

Fig. 5

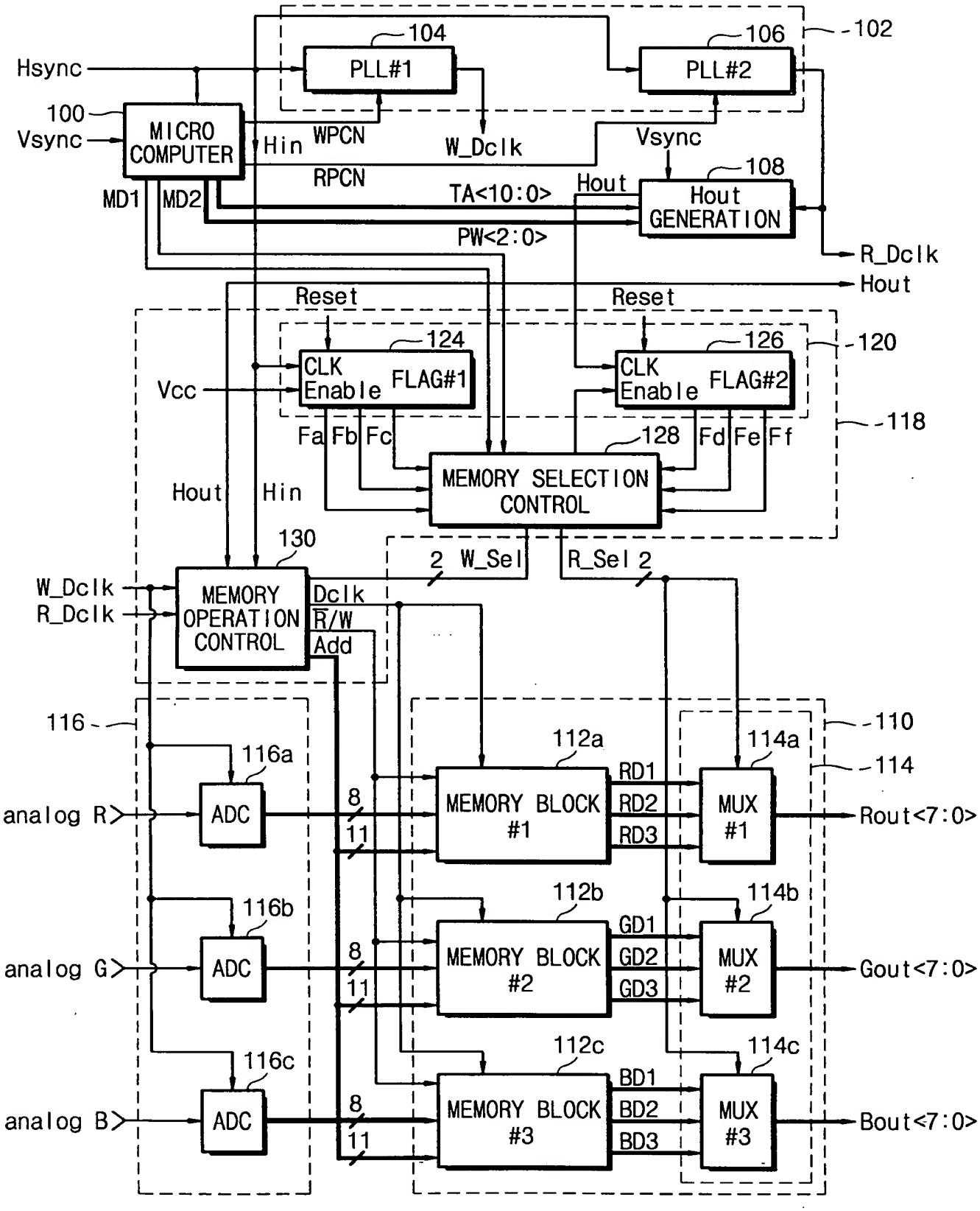

Hsync
100
Vsync
MICRO COMPUTER
104
PLL#1
106
PLL#2
102
Hin
WPCN
W_Dclk
RPCN
Vsync
108
Hout GENERATION
TA<10:0>
Hout
MD1
MD2
PW<2:0>
R_Dclk
Hout
Reset
Reset
124
CLK Enable FLAG#1
126
CLK Enable FLAG#2
120
Vcc
118
Fa Fb Fc
128
Fd Fe Ff
MEMORY SELECTION CONTROL
Hout
Hin
130
2 W_Sel
R_Sel 2
W_Dclk
R_Dclk
MEMORY OPERATION CONTROL
Dclk
R/W
Add
116
116a
112a
114a
110
114
analog R
ADC
8
11
MEMORY BLOCK #1
RD1
RD2
RD3
MUX #1
Rout<7:0>
116b
112b
114b
analog G
ADC
MEMORY BLOCK #2
GD1
GD2
GD3
MUX #2
Gout<7:0>
116c
112c
114c
analog B
ADC
MEMORY BLOCK #3
BD1
BD2
BD3
MUX #3
Bout<7:0>

Fig. 6

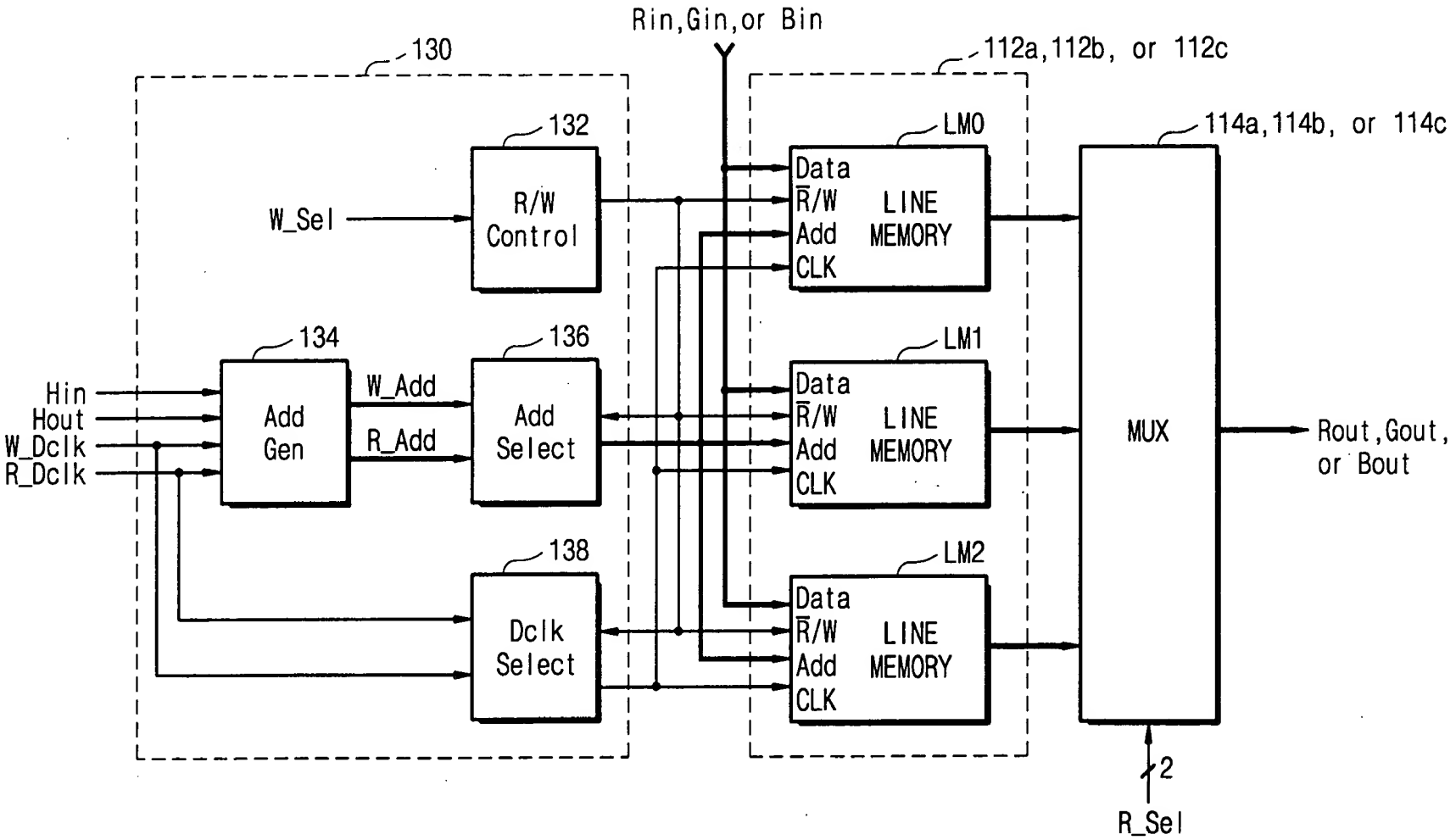

Rin,Gin,or Bin
130
112a,112b, or 112c
132
LM0
114a,114b, or 114c
W_Sel
R/W Control
Data
R/W
Add
CLK
LINE MEMORY
134
136
LM1
Hin
Hout
W_Dclk
R_Dclk
Add Gen
W_Add
R_Add
Add Select
MUX
Rout,Gout, or Bout
138
LM2
Dclk Select
2
R_Sel

Fig. 7

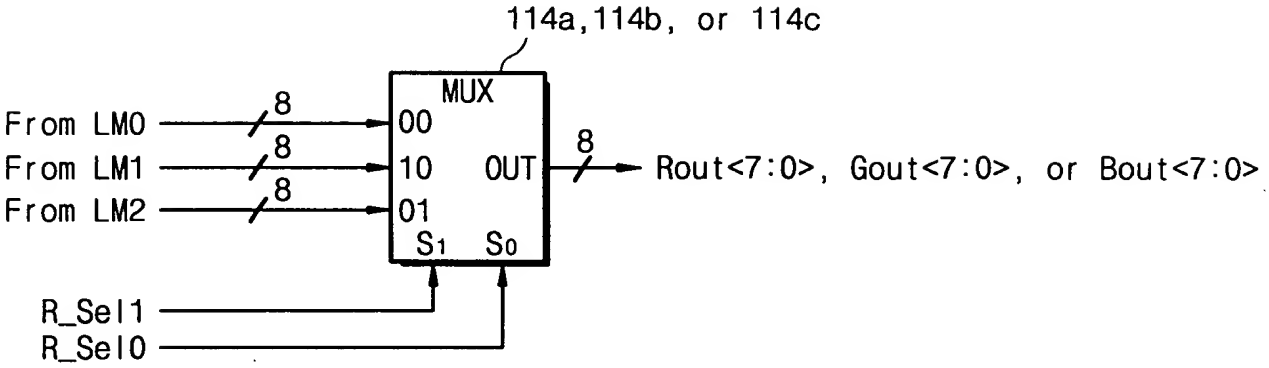


Fig. 8

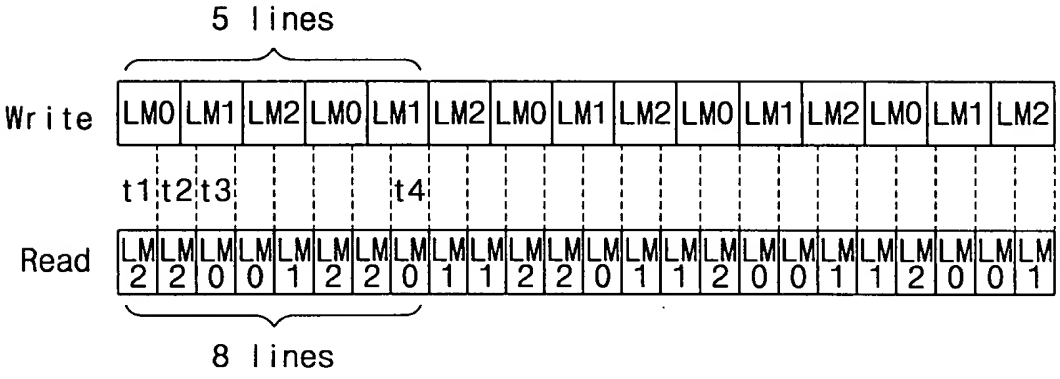


Fig. 9

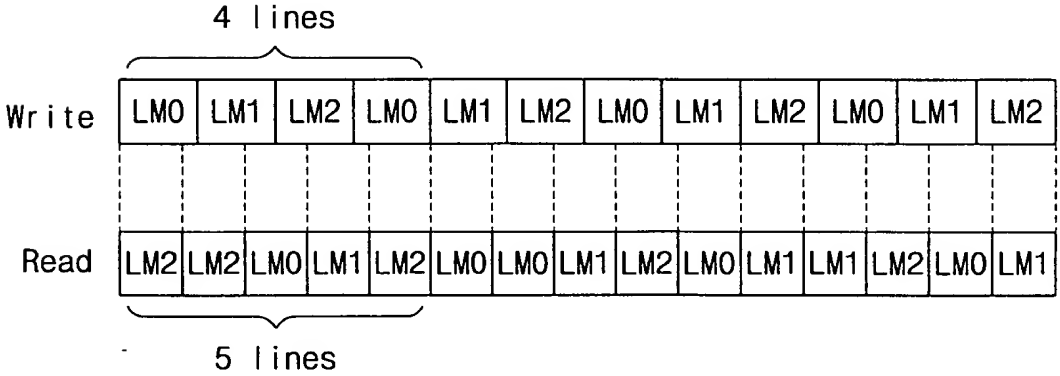


Fig. 10

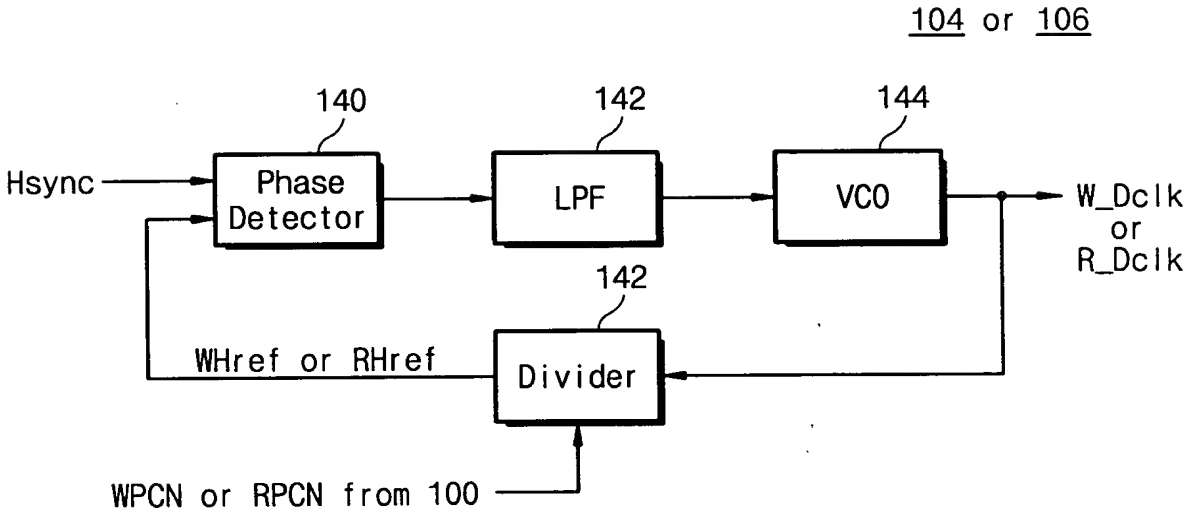

104 or 106
140
142
144
Hsync
Phase Detector
LPF
VCO
W_Dclk or R_Dclk
142
WHref or RHref
Divider
WPCN or RPCN from 100

Fig. 11

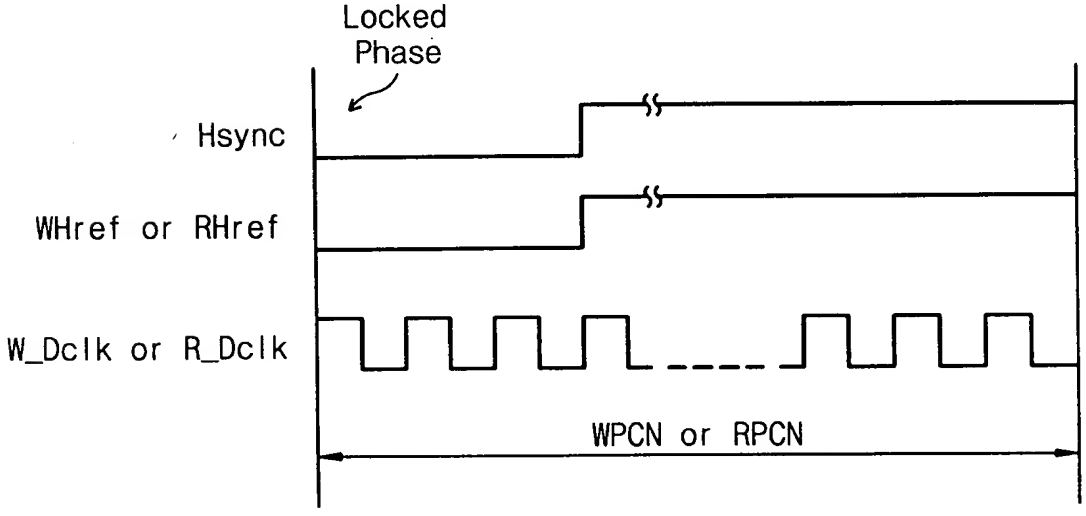

Locked Phase
Hsync
WHref or RHref
W_Dclk or R_Dclk
WPCN or RPCN

Fig. 12

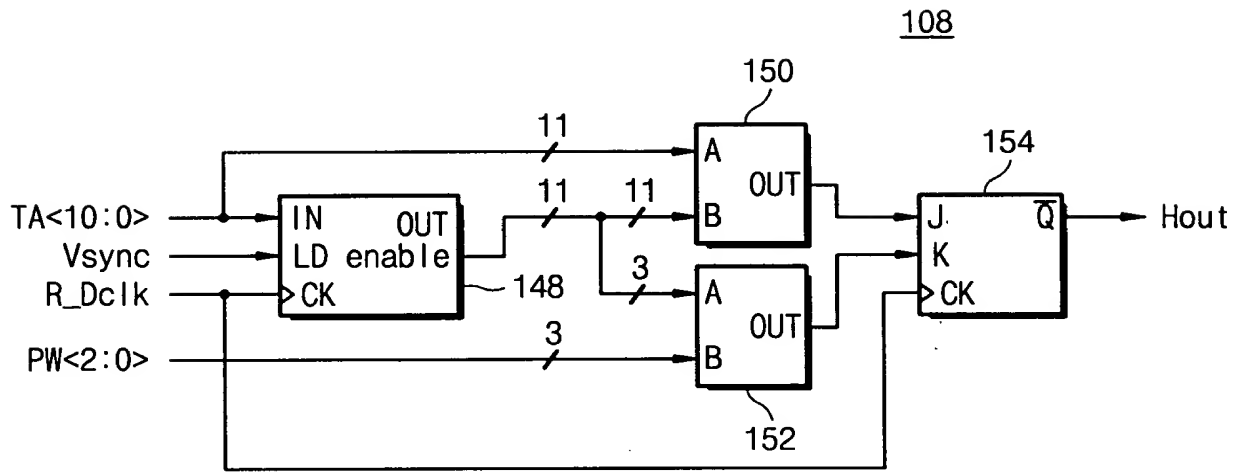

108
150
154
11
11
11
3
3
A
B
OUT
IN
LD enable
CK
148
J
K
Q
TA<10:0>
Vsync
R_Dclk
PW<2:0>
Hout
152

Fig. 13

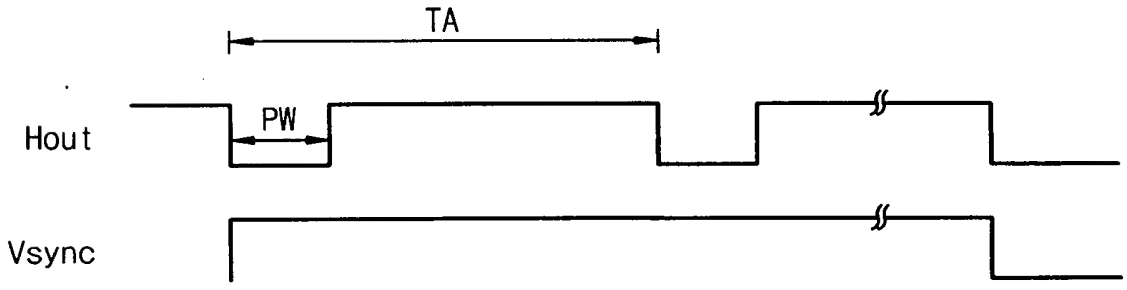

TA
PW
Hout
Vsync

Fig. 14

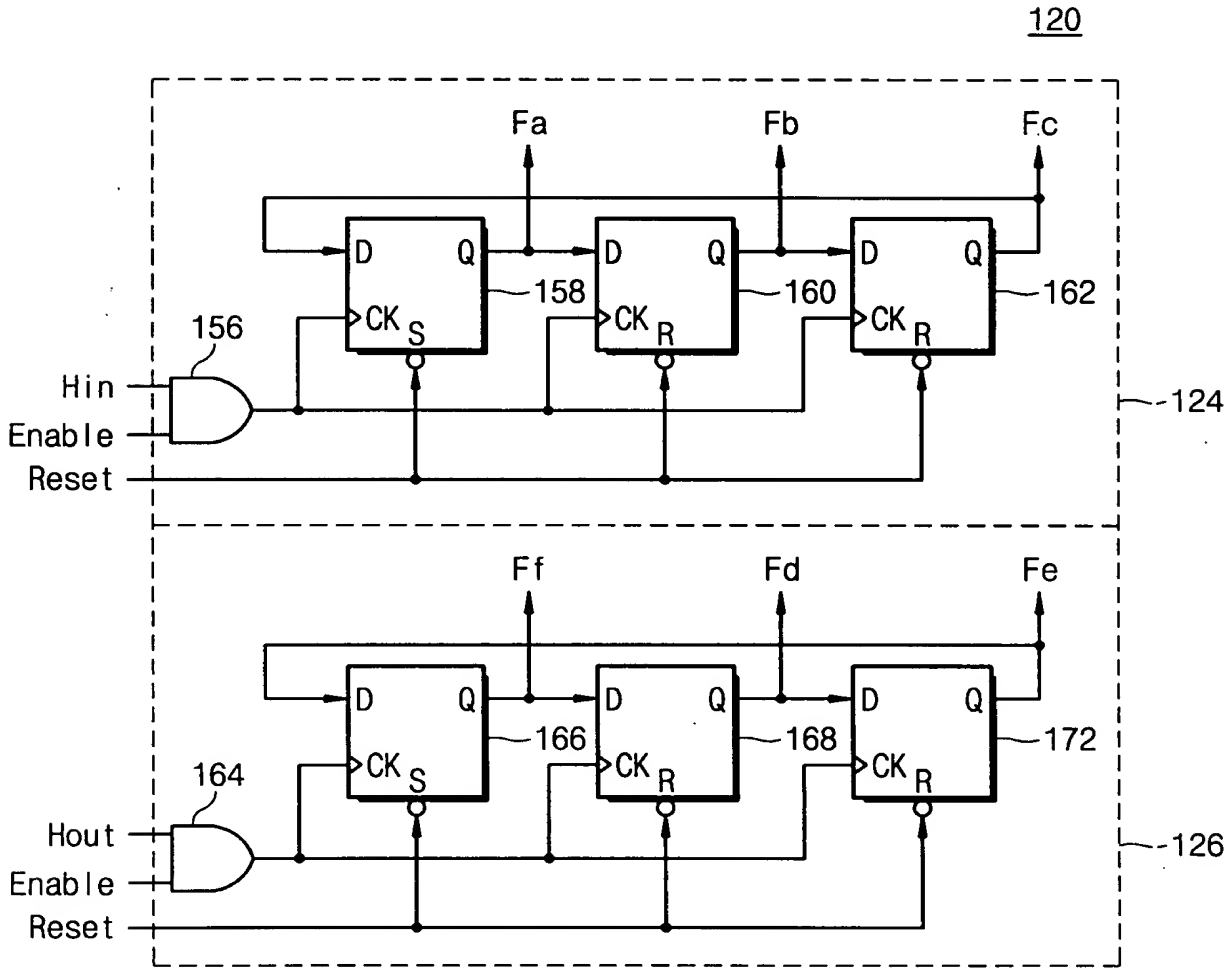

120
Fa
Fb
Fc
D
Q
CK
S
R
158
160
162
156
Hin
Enable
Reset
124
Ff
Fd
Fe
166
168
172
164
Hout
Enable
Reset
126

Fig. 15

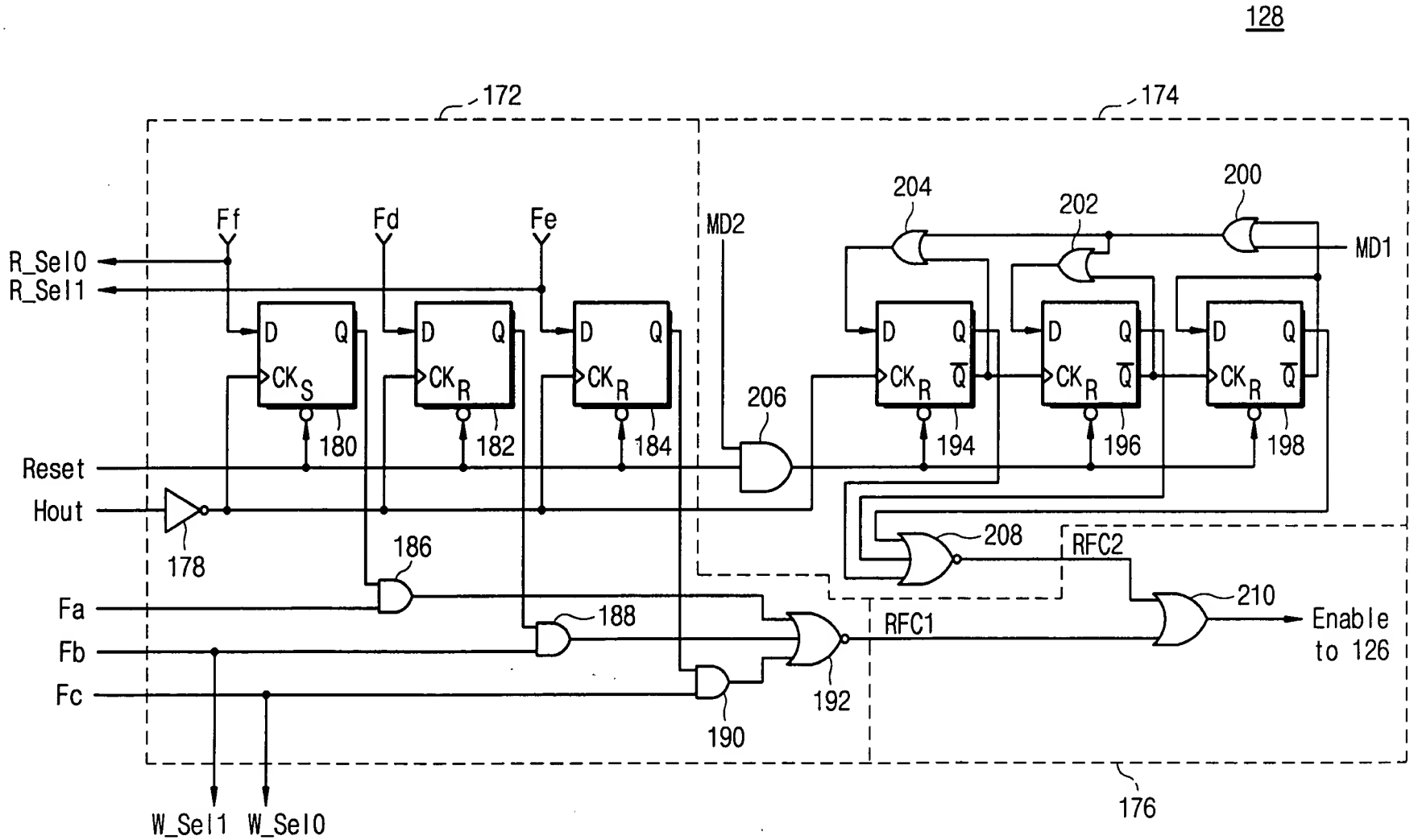

128
172
174
Ff
Fd
Fe
MD2
204
202
200
MD1
R_Sel0
R_Sel1
D
Q
CK_S
CK_R
180
182
184
206
194
196
198
Reset
Hout
178
186
208
RFC2
210
Fa
Fb
Fc
188
RFC1
Enable to 126
192
190
W_Sel1
W_Sel0
176

Fig. 16

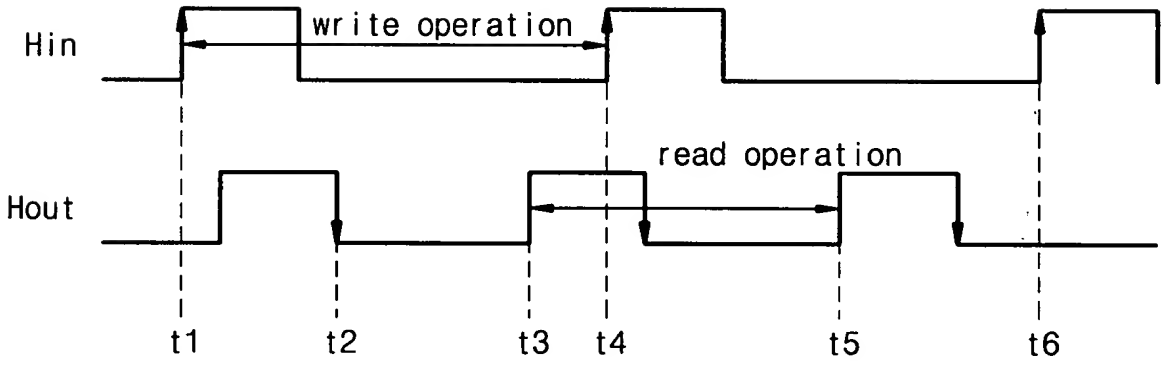
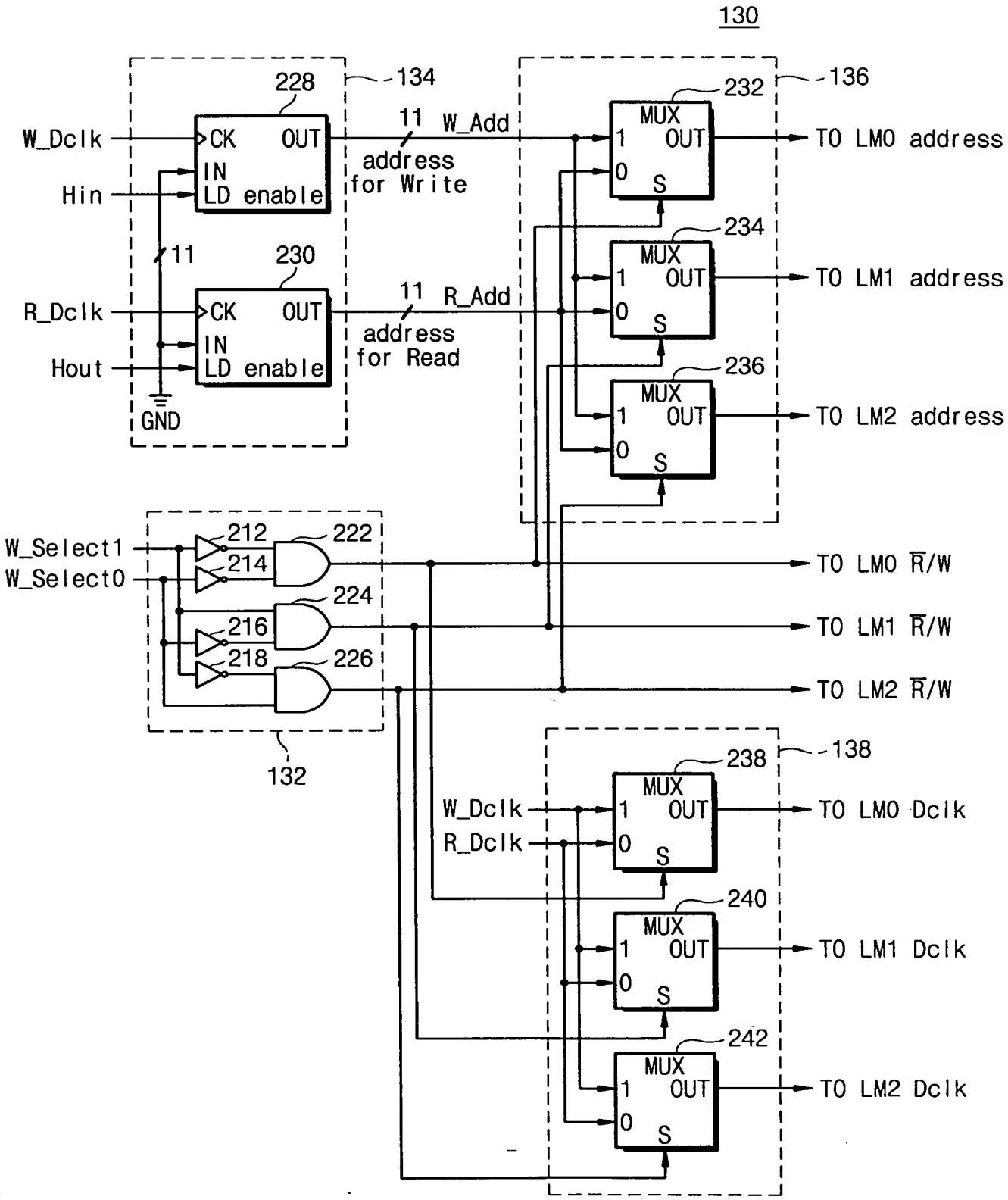


Fig. 17


130
134
136
228
230
232
234
236
W_Dclk
Hin
R_Dclk
Hout
GND
CK
OUT
IN
LD enable
11
W_Add
address for Write
R_Add
address for Read
MUX
1
0
S
TO LM0 address
TO LM1 address
TO LM2 address
W_Select1
W_Select0
212
214
216
218
222
224
226
132
TO LM0 R/W
TO LM1 R/W
TO LM2 R/W
138
238
240
242
TO LM0 Dclk
TO LM1 Dclk
TO LM2 Dclk